⑫ # EUROPEAN PATENT APPLICATION

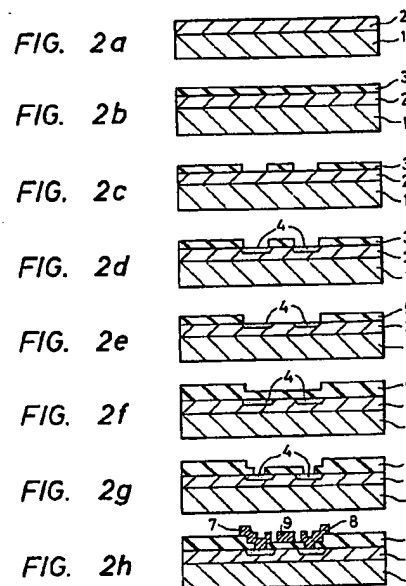⑦ Applicant: Hitachi, Ltd., 5-1, Marunouchi 1-chome,
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㉔ Polycrystalline thin-film transistor integrated circuit including such transistors and a display device including such a circuit.

㉗ A polycristalline thin-film transistor has a polycristalline silicon layer 2 formed on a substrate 1. The layer 2 includes at least a pair of electrode-contacted regions 4 for causing carriers to migrate, and there are means for controlling the carriers. In order to achieve high uniformity of characteristics among the different transistors in the layer, the length of the region in which the carriers migrate is at least 10 times greater than the mean grain size of the silicon in the general migration direction of the carriers, and the mean grain size in at least the region in which the carriers migrate is not less than 150 nm. Preferably, the ratio between the coefficients of thermal expansion of the substrate and the polycrystalline silicon layer is in the range 0.3 to 3.0.

FIG. 2a

FIG. 2b

FIG. 2c

FIG. 2d

FIG. 2e

FIG. 2f

FIG. 2g

FIG. 2h

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"Polycrystalline thin-film transistor integrated
circuit including such transistors and a
display device including such a circuit"

The present invention relates to a tran-
sistor the material of which is a polycrystalline
semiconductor layer formed on an insulating body
and further relates to a semiconductor integrated
5   circuit including a plurality of such transistors
and to a display device including such a circuit.
The transistor of the present invention
is useful as, for example, a semiconductor device
which is unitary with the displaying substrate
10 of a flat display device employing a liquid crystal,
electroluminescence or the like and which is operated
to drive the display device.
In a flat display device employing a
liquid crystal, there has hitherto been adopted
15 a system in which, on for example a single-crystal
Si substrate, there is formed an integrated circuit
in which a two-dimensional switching matrix of
MOS transistors and peripheral scanning circuitry
are unitary. The liquid crystal, which fills up
20 the interspace between the single-crystal Si

integrated circuit elements and counter electrodes,

is driven by those circuit elements. Since the

substrate is a single crystal, the size of the

substrate which can be prepared is limited, and

5 hence the size of the screen of the liquid-crystal

flat display device is limited. By way of example,

the diameter of a Si wafer which can be produced

at present is at most 5 inches, so that a screen

of a size corresponding to a cathode-ray tube larger

10 than the 5-inch type cannot be fabricated. It

is a serious disadvantage as a picture device that

a large area cannot be attained.

To the end of eliminating this disadvantage,

it has also been proposed that an amorphous semi-

15 conductor layer or a polycrystalline semiconductor

layer is formed on an amorphous substrate, and

integrated circuit elements as described above

are formed using the material of this layer and

are used to drive a flat display device. Since,

20 in this case, the semiconductor layer may be formed

on the amorphous substrate by a process such as

vacuum evaporation, a large area in excess of a

diameter of 5 inches can be attained, and the area

of the flat display device can be made large.

25

However, the carrier mobility of the
amorphous semiconductor layer is conspicuously
low, and the characteristics of the transistors
formed of it are inferior. On the other hand,
5 in a polycrystalline semiconductor layer, the carrier
mobility is high enough for use as the display
device. However, if the grain size and the current
path (channel) length of the element are approximately
equal, the presence of a grain boundary leads to
10 the disadvantage that the characteristics of the
respective elements vary. More specifically,
the current path of one element traverses the grain
boundary, whereas the current path of another
element does not, and the conduction of carriers
15 is affected by the grain boundary in some elements
and not in the others. As a result, the individual
elements differ in their transistor characteristics,
for example, the transconductance.

Examples of polycrystalline silicon devices,
20 are described in the following references:

(1) THIN-SOLID FILMS, vol. 35, June 1976, no.
2, pp. 149-153

(2) ELECTRICAL DESIGN NEWS, vol. 18, no. 13, July
1973, pp. 30-31

25 (3) IBM TECHNICAL DISCLOSURE BULLETIN, vol. 14,
no. 10, March 1972, pp. 2900-2901

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(4) Applied Physics Letters, vol. 35, 15th July

     1979, no. 2, pp. 173-175

(5) IBM TECHNICAL DISCLOSURE BULLETIN, vol. 17,

     no. 8, January 1975, pp. 2455-2456

5   (6) SOLID STATE ELECTRONICS, vol. 15, no. 10,

     October 1972, pp. 1103-1106

        An object of the present invention is

to eliminate or mitigate the disadvantages of the

prior art described above and to provide a thin-

10 film transistor having excellent and more uniform

transistor characteristics.

        The present invention is set out in the

claims.

        An embodiment of the invention will now

15 be described by way of example with reference to

the accompanying drawings, in which:-

        Figure 1 is a graph showing the relation-

ship between the thickness of an evaporated layer

and the grain size;

20   Figures 2a - 2h are sectional views showing

a process for producing a MOSFET embodying the

present invention, by the use of a polycrystalline

semiconductor layer;

        Figure 3 is a characteristic diagram

25 of a MOSFET of an embodiment of the invention; and

Figure 4 is a graph showing the relationship

between the mean grain size and the transconductance.

In the invention, a polycrystalline

semiconductor layer is formed on a predetermined

5   substrate and a semiconductor device is formed

using the polycrystalline semiconductor layer.

The length of a path in which carriers move (the

channel length) is equal to or greater than 10

times the grain size (the longer diameter when

10   a crystal grain is flat). In this specification,

the term "grain size" signifies the "mean grain

size". More specifically, the characteristics

of the circuit elements depend upon the number

of grain boundaries which the carriers encounter

15   in the course of migration (travel). Since there

are a sufficiently large number of crystal grains

in the carriers path, each carrier is affected

by a large number of grain boundaries. Therefore,

when a large number of semiconductor devices are

20   manufactured, their characteristics have a good

uniformity. To minimize variation of the character-

istics, it is preferable that the length of the

path in which the carriers move is equal to or

greater than 50 times the grain size.

25

On the other hand, if the grain size

is too small, the characteristics (for example,

the mobility of carriers) of the semiconductor

material as a whole are inferior, so that the grain

5   size should preferably be at least 150 nm.

Of course, even when the grain size is

smaller than this value, the relationship between

the length of the travel path of the carriers and

the grain size is useful in reduction of the variation

10   of the characteristics of the elements and in rendering

the elements uniform.

A semiconductor layer having a mean grain

size of or below approximately 300 nm is easily

made. It can be satisfactorily realised and controlled

15   by evaporation in ultra-high vacuum, as described

later.

If the length of the travel path of carriers

(in, for example, a field effect transistor, this

length corresponds to the channel length) is

20   determined in the circuit design of a semiconductor

device in advance, the polycrystal grain size is

adjusted. On the other hand, if the grain size

is limited by any restriction on the conditions

of forming the polycrystalline layer, the elements

25   and the circuit need to be designed in conformity

with the limited grain size.

The length of the (travel path) ranging region of the carriers has no upper limit in theory, but it will be at most 100 µm in practice. In

5   addition, although the lower limit of the grain size is difficult to set specifically, the mobility of the carriers can be secured with grain sizes of at least 100 Å in practice. Accordingly, the ratio between the length of the travel path of

10 the carriers and the grain size may be 10000 or so at its upper limit in practice.

The thickness of the semiconductor layer is preferably at least 100 nm because a channel may be formed in the layer. A thickness of at

15 least 500 nm is more preferred.

Useful as the substrate is an amorphous or polycrystalline substrate such as a glass or ceramics substrate. One factor is price. Particularly the glass substrate is inexpensive. Furthermore,

20 it is possible to use a light-transmitting substrate.

It is preferred in order to obtain semi- conductor devices of slight variation, that the ratio (C_{sub}/C_{semi}) between the coefficient of thermal expansion (C_{sub}) of the substrate and the coefficient

25 of thermal expansion (C_{semi}) of the semiconductor

material is within the range 0.3 to 3.0. Although

the details of the physical reasons are not clear,

this requirement derives from the stressed state

of the semiconductor layer attributed to the difference

5 of the coefficients of thermal expansion of the

substrate and the semiconductor layer.

A preferred method of evaporating a suitable

polycrystalline semiconductor layer is now described.

The vacuum evaporator used is capable

10 of attaining ultra-high vacuum, and may be a

conventional evaporator having an ultra-high vacuum

device. The degree of vacuum during the evaporation

is kept below 1×10^{-8} Torr. Particularly O_2 present

in the residual gas during the evaporation has

15 bad effects on the characteristics obtained, so

that the partial pressure of oxygen is kept below

1×10^{-9} Torr.

The evaporation rate is in the range

1,000 Å/hour to 10,000 Å/hour.

20 Control of the grain size can be accomplished

by controlling one or more of the thickness of

the evaporated layer, the temperature of the substrate,

the rate of evaporation and the degree of vacuum.

Figure 1 is a graph showing the relationship between

25 the thickness of an evaporated silicon layer and

the mean grain size thereof, the layer having been

evaporated under the conditions of a substrate

temperature of 600°C, an evaporation rate of 5000

Å/hour and a degree of vacuum during evaporation

of 8×10^{-9} Torr. The thickness of the layer was

5   measured with a quartz oscillator.

In some cases, the grain size may be

controlled by such techniques as laser annealing.

In order to fabricate a semiconductor

device by processing a polycrystalline silicon

10   layer, several manufacturing steps must be performed.

The heat-treatment temperatures in these steps

should be kept below 820°C which is the softening

point of very hard glass, in order that the advantages

obtainable with the present invention can be fully

15   exploited. If employing a glass substrate of low

softening point, the heat-treatment temperatures

should be kept still lower, for example, below

550°C. In the following, there will be exemplified

a case where a MOS field effect transistor is formed

20   on a glass substrate of low softening point.

In producing a gate insulator, the technique

of thermal oxidation of a silicon substrate is

ordinarily used. Since, however, this thermal

oxidation requires a temperature of at least 1000°C,

25   it cannot be used here. In this example, SiH_4

and O_2 are reacted at a temperature of 300°C to

at most 500°C, or SiH_4 and NO_2 are reacted at a

temperature of 400°C to at most 800°C, to form

an SiO_2 film by chemical vapor deposition. This

5   SiO_2 film is used as the gate insulator.

To form a source region and a drain region,

the method of forming p^+ layers or n^+ layers by

thermal diffusion has hitherto usually been performed,

but this requires a heat treatment at about 1150°C

10   and cannot be used for the present purpose of forming

a transistor on a glass substrate of low softening

point. In the present embodiment thermal diffusion

is replaced by the method of forming p^+ layers

or n^+ layers by ion implantation. After ion implant-

15   ation, a heat treatment for electrical activation

is performed, in which the temperature needs to

be kept lower than the softening point of the substrate

used. Therefore, there is adopted, for example,

a method in which ions such as BF_2^+ permitting

20   high activation through a heat treatment at a low

temperature of about 550°C are implanted, or a

method in which, after ions such as B^+ are implanted,

a heat treatment is performed at a temperature

of about 500°C-600°C immediately before the reverse

25   annealing effect takes place. With P^+ ions, As^+

ions etc., the reverse annealing effect is not

so remarkable as in the case of the B^+ ions, but

such impurities can be satisfactorily activated

by heat treatment at about 500°C-600°C. Accordingly,

5   both a p^+ layer and an n^+ layer can be formed by

a low-temperature process at about 500°C-600°C.

When employing a substrate, such as a very hard

glass, whose softening point is higher than 800°C,

there may of course be used a heat treatment at

10   800°C.

By the manufacturing method described

above, the semiconductor layer can be made large

in area or elongate, and a semiconductor material

having a carrier mobility of at least 1 cm^2/V.sec

15   can be produced.

Referring to sectional views of Figures

2a - 2h which illustrate the steps of manufacture,

there will be described as an embodiment of the

invention, the fabrication of an n-channel MOS

20   field effect transistor in which a polycrystalline

silicon layer is formed on a glass substrate and

a channel is provided in the surface layer of the

polycrystalline silicon layer.

First, the substrate is placed within

25   a vacuum evaporator which can achieve ultra-high

vacuum. The evaporator may be a conventional one.

On the glass substrate 1 (aluminosilicate glass;

coefficient of thermal expansion = 32 x 10^{-7}/°C)

a silicon layer 2 is deposited to a thickness of

5 1.5 μm by vacuum evaporation under the conditions

of a substrate temperature of 600°C, a degree of

vacuum during evaporation of 8 x 10^{-9} Torr and

an evaporation rate of 5000 Å/hour (Figure 2a).

The silicon layer 2 formed is of p-type poly-

10 crystalline silicon which is slightly doped with

boron and which has a grain size of about 2000

Å and a carrier mobility of about 2 cm^2/V.sec.

The coefficient of thermal expansion of this silicon

layer is about 25 x 10^{-7}/°C (300 °K).

15   Subsequently, an SiO_2 film 3 is deposited

to a thickness of 5000 Å by vapor growth at a substrate

temperature of 400°C (figure 2b). Next, as shown

in Figure 2c, the SiO_2 film 3 is provided with

windows for source and drain regions. The gap

20 between the source region and the drain region

is made 20 μm, so that the channel length of the

MOS field effect transistor is also 20 μm. Subsequently

p^+ ions having energy of 100 keV are implanted

at a dose of 1 x 10^{16}/cm^2, and the resultant substrate

25 is heat-treated in an N_2-atmosphere at 600°C for

30 minutes, whereby n^+ layers 4 are formed in the

source and drain regions (Figure 2d).

At the next step, as shown in Figure

2e, the SiO_2 is removed with a field oxide film

5   5 left behind. An SiO_2 film 6 is deposited as

a gate oxide film to a thickness of 7500 Å by chemical

vapor deposition (Figure 2f) and electrode contact

holes are provided as shown in Figure 2g by photo-

etching. After Al has been evaporated onto the

10 whole surface, it is processed by photoetching

to form a source electrode 7, a drain electrode

8 and a gate electrode 9 (Figure 2h). Thereafter,

the product is heat-treated in an H_2-atmosphere

at 400°C for 30 minutes.

15   By these steps, a thin-film MOS field

effect transistor with the structure in which

the channel 20 μm long is provided in the surface

layer of the polycrystalline silicon layer has

been fabricated. This semiconductor device exhibits

20 good and stable transistor characteristics.

Figure 3 shows an example of the character-

istic, at room temperature, of a MOSFET which was

manufactured in this way by way of trial. The

characteristic shown is the drain current I_D-versus-

25 drain voltage V_{DS} characteristic with a parameter

being the gate voltage V_G.

In this example, the grain size is approximately 2000 Å with respect to the channel length of 20 μm. Accordingly, a sufficiently large

5 number of crystal grains exist in the travel direction of carriers, and the carriers are each influenced by a large number of grain boundaries. Consequently, when a large number of elements are manufactured, their characteristics become uniform.

10 Silicon layer having various mean grain sizes were formed, and semiconductor devices similar to that described above were manufactured. The transconductances of the devices were compared, and the results are illustrated in Figure 4, in

15 which the transconductances are given relative to the typical value of the transconductance of a layer having a grain size of 150 nm which is made unity. It will be seen that when the mean grain size is less than 150 nm, the transconductance

20 is reduced sharply.

MOS field effect transistors having various gate lengths were manufactured using semiconductor layers whose mean grain sizes were 150 nm, 200 nm and 300 nm, and the (dispersion) variations

25 in each case of the transconductances of the

transistors were tested. When the ratio of the
travel distance of carriers to the mean grain size
was below 10 times, a dispersion on the order of
$\binom{+3}{-1}$ was exhibited with respect to transconductance

5   (relative value) = 1. The condition of transconductance
= 0 signifies that operation is, in effect, impossible.

On the other hand, when the ratio of
travel distance to mean grain size was 10 times
to 50 times, the dispersion was of the order of

10 ± 0.7 to ± 0.8, and when this ratio exceeded 50
times, the dispersion was of the order ± 0.3 to
± 0.4. Even when the ratio was approximately 200
times to 1000 times, the dispersion was of the
order of ± 0.3 to ± 0.4.

15   Similar MOS field effect transistors
were manufactured using various substrates, and
their transconductances (g_m) were measured. The
results are listed in Table 1. In the manufacture,
heat treatments were carried out at temperatures

20 not higher than 500°C. With quartz glass or soda-
lime glass, no transistor having good characteristics
can be produced. The ratio between the coefficients
of thermal expansion of the substrate and the semi-
conductor layer placed thereon should preferably

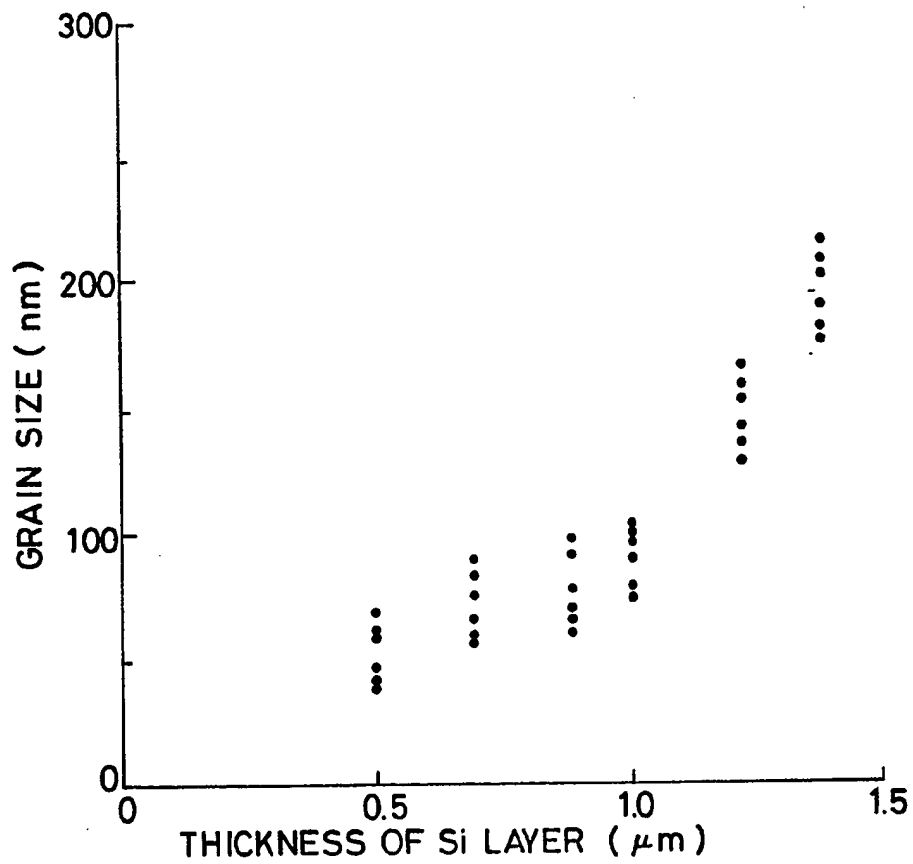25 be set within predetermined limits, as discussed
above.

TABLE   1

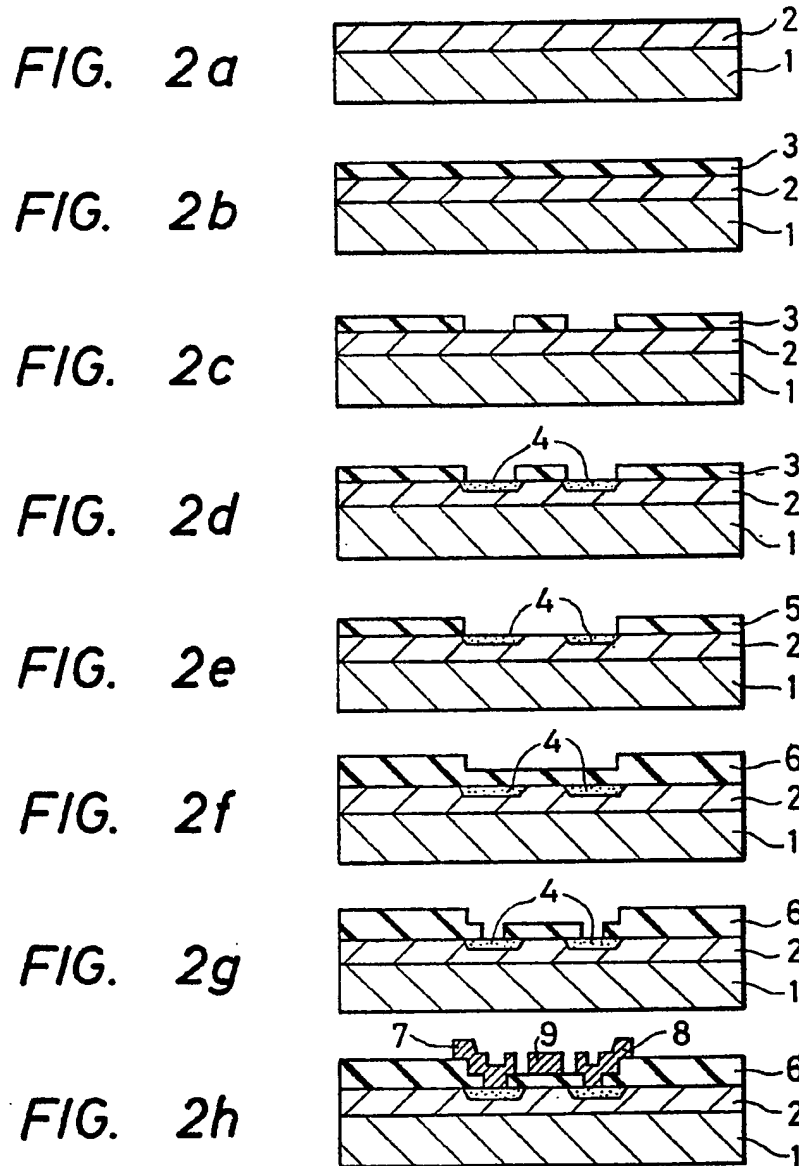| Substrate	Coefficient of thermal expansion of substrate (0 to 300°C) x 10^{-7})	Ratio $= \dfrac{Co(Sub)}{Co(Semi)}$	g_m (V_G=10V)
quartz glass	5.5	0.22	1 to 9 µs
boro- silicated glass (I)	32	1.28	10 to 50 µs
boro- silicated glass (II)	46	1.84	10 to 100µs
boro- silicated glass (III)	50	2.0	10 to 100µs
alumino- silicate glass	54	2.16	10 to 100µs
soda-lime glass (I)	87	3.48	-
soda-lime glass (II)	94	3.76	-

CLAIMS:

1.   A polycrystalline thin-film transistor
wherein a polycrystalline silicon layer (2) is
formed on a substrate (1), the polycrystalline
silicon layer (1) including at least a pair of
5   electrode regions (4) for causing carriers to migrate,
and there being means (7,8,9) for controlling the
carriers
characterized in that
the length of the region in which the carriers
10 migrate is at least ten times greater than the
mean grain size of the polycrystalline silicon
in the general migration direction of the carriers,
the said mean grain size in at least the said region
in which the carriers migrate is not less than
15 150 nm.

2.   A polycrystalline thin-film transistor
according to claim 1, wherein the said length of
the region in which the carriers migrate is at
least 50 times greater than the said mean grain
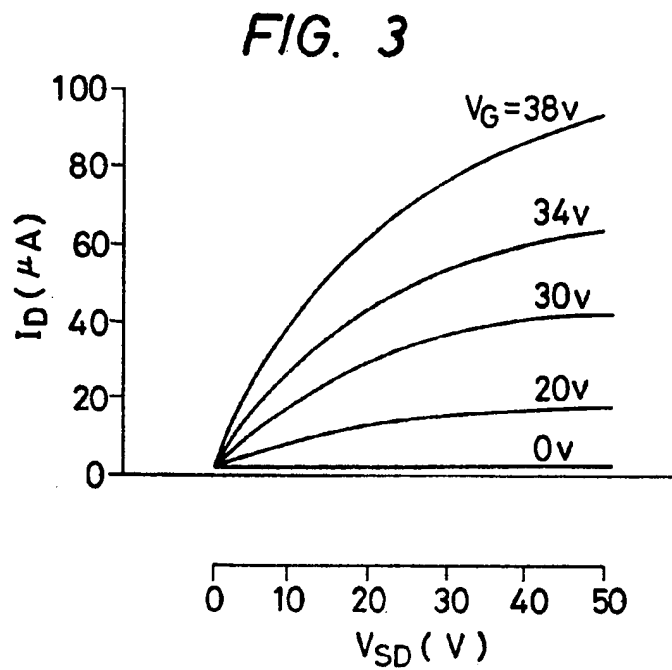20 size in the general migration direction of the
carriers.

3.   A polycrystalline thin-film transistor
according to claim 1 or claim 2 wherein the ratio
between the coefficients of thermal expansion of
the substrate and of the polycrystalline silicon
5   layer is in the range 0.3 to 3.0.

4.   A polycrystalline thin-film transistor
according to any one of claims 1 to 3 wherein said
polycrystalline silicon layer is a polycrystalline
film formed by vacuum evaporation in ultra-high
10   vacuum.

5.   A semiconductor integrated circuit including
a plurality of transistors according to any one
of claims 1 to 4 included in a single said poly-
crystalline layer (2).

15 6.   A display device including a semiconductor
integrated circuit according to claim 5.

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FIG. 1

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FIG. 2a

FIG. 2b

FIG. 2c

FIG. 2d

FIG. 2e

FIG. 2f

FIG. 2g

FIG. 2h

FIG. 3

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FIG. 4